

REMARKS

In the Office Action, Claims 1, 3-6, and 8-27 were examined and are rejected. In response, Claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1, 3-6, and 8-27 in view of the following remarks.

I. Objection to the Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. It is asserted that the claimed subject matter in claims 6 and 8-10 is not supported by the specification, which fails to define “a computer readable storage medium.”

Claims 6 and 8-10, as filed, recited “an article of manufacture including a machine-readable medium ...” We submit that memory 440 (FIG. 10) is a machine-readable storage medium. As currently amended, Claims 6 and 8-10 recite “a machine-readable medium.” In view of the amendment, please withdraw the objection to the specification.

I. Claims Rejected Under 35 U.S.C. §102

Claims 1, 3-6, and 8-26 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,275,891 to Dao et al. (“Dao,” previously cited). Applicants respectfully traverse this rejection.

Claim 1 recites:

1. A method comprising:
detecting an update to a register file accessible by a plurality of processing elements of a media signal processor when a processing element desires ownership of a selected hardware accelerator;
enabling the hardware accelerator selected from a plurality of hardware accelerators in response to one or more address bits and a control command detected within a register within the register file that are written by the processing element to identify and request ownership of the selected hardware accelerator; and
granting the processing element ownership over the selected hardware accelerator, the selected hardware accelerator to perform a media processing function according to the detected control command. (Emphasis added.)

Dao is generally directed to a system for multimedia processing, where a data traffic master provides shared memory connections to one or more processing units. (See Abstract.) FIG. 2 of Dao describes an architecture that includes three portions, a memory portion 202, a data portion (traffic master) 204, and a processor portion 206. (See col. 3, lines 38-40.) The traffic master of Dao coordinates all inter-processor, inter-memory, and processor-memory communications subject to programmed privileges to the page-based shared memory 322. (See col. 4, lines 4-8 and col. 5, lines 22-28.) Dao further indicates that processor units assert an enable signal to send or receive data. When the traffic master is ready to transfer or receive data, the traffic master asserts a ready signal. (See col. 4, lines 44-56.)

In contrast with Claim 1, Dao does not disclose detecting an update to a register file, accessible by a plurality of processing elements of a media signal processor, when a processing element desires ownership of a selected hardware accelerator. Dao does describe a mailbox message communication between processors (see col. 6, lines 57-60). Dao describes a memory management unit (MMU) (see col. 5, lines 65-67) and registers that are part of a logically mapped memory space that is used by the processors to perform the mailbox message communication between the processors.

Dao indicates that when a processor attempts to write to an MMU without write permission, an ICU 412 can assert and interrupt to alert one of the processors of the memory protection violation. (See col. 6, lines 37-40 and 64-65.) However, assertion of the interrupt is different from detecting a register file update when a processing element desires ownership of a selected hardware accelerator, as in Claim 1.

Furthermore, Dao does not disclose or suggest enabling a hardware accelerator in response to one or more address bits and a control command detected within a register within a register file that are written by a processing element to identify and request ownership of the selected hardware accelerator, as in Claim 1. According to the Examiner, Dao discloses that when a processor unit (e.g., a DSP) desires to access another processor unit (such as hardware accelerator) through the traffic master 204, the request processor unit should provide (besides address and data) an enable signal. (See col. 4, lines 32-53.) (See page 3, para. 2 of the Office Action mailed 1/22/08.) However, the passages indicated by the Examiner refer to the sending

or receiving of data by the array of processors 206 to and from the various memory shown, for example, as part of shared memory 202/322, as shown in FIGS. 2 and 3. However, the sending/receiving of data by the array of processors 206 to/from shared memory 322 is different from enabling of a selected hardware acceleration in response to one or more address bits and a control command detected within a register file that are written by a processing element to identify and request ownership of a selected hardware accelerator, as in Claim 1.

The assertion of a ready signal by traffic master 204 for handling the sending/receiving of data between processors 206 and shared memory 322 does not disclose granting the processing element ownership over the selected hardware accelerator, the selected hardware accelerator to perform a media processing function according to the detected control command, as in Claim 1.

As indicated by the Examiner, Col. 8, lines 15-32 of Dao show that DSP modify (update) the registers of the mailbox, when the DSP 320 desires ownership of the selected hardware accelerator 318 to perform the IDCT, granting the processing element (DSP 320) the ownership over the selected hardware accelerator at 318 at the request of the processing element (see page 9 of the Office Action mailed August 6, 2008). However, the passage referred to by the Examiner describes a situation where a microcontroller 104 downloads an encoded video macro block to a DSP memory 202e. As described, the microcontroller 104 writes a message to the DSP's mailbox. As further indicated by such passage, the DSP 320 receives the message and decodes the video macro block with the results written to the hardware accelerator's memory (202g).

In this example described by Dao, there is no request of ownership of hardware accelerator 318 since the DSP 320 simply writes the results to the hardware accelerator's memory without any request for ownership over the hardware accelerator. Furthermore, when the DSP 320 sends a message to the hardware accelerator's mailbox to begin the inverse discrete cosine transform, we submit that this mailbox message merely directs the hardware accelerator to begin the transformation of the decoded macro block. This mailbox message is not a request for ownership and certainly does not disclose the enabling of a hardware accelerator in response to one or more address bits and a control command detected within a register within a register file that are written by a processing element to identify and request ownership of the selected hardware accelerator, as in Claim 1.

Furthermore, as indicated by the passage referred to by the Examiner, upon completion, the accelerator sends a message to the MCU 104 requesting a transfer of the decoded video block to the video buffer. We submit that the lack of any communication between the accelerator and DSP 320 prohibits the Examiner from establishing that the DSP is granted ownership over the hardware accelerator, as in Claim 1. The disclosure of Dao is expressly limited to the ability of the DSP to write the results of some decoding algorithm (performed on an encoded video macro block with the results written) to a hardware accelerator's memory.

The writing of results to a hardware accelerator's memory and the subsequent transmission of a message to the accelerator's mailbox to begin decoding cannot properly be interpreted as disclosing the enabling the selected hardware accelerator from a plurality of hardware accelerators in response to one or more address bits and a control command detected within a register within a register file that are written by a processing element to identify and request ownership of the selected hardware accelerator, as in Claim 1. We submit that the hardware accelerator referred to by Dao would already be enabled and hence does not become enabled in response to one or more address bits of a register within a register file that are set by a processing element to identify and request ownership of the selected hardware accelerator, as in Claim 1.

Hence, the Examiner has failed to identify, and we are unable to discern, any portion of Dao that discloses or suggests enabling the hardware accelerator selected from a plurality of hardware accelerators in response to one or more address bits and a control command detected within a register within a register file that are written by a processing element to identify and request ownership of the selected hardware accelerator, much less granting the processing element ownership over the selected hardware accelerator, the selected hardware accelerator to perform a media processing function according to the detected control command, as in Claim 1.

For each of the above reasons, Claim 1, and all claims which depend from Claim 1, are patentable over the cited reference Dao as well as the references of record.

Each of Applicants' other independent claims, including Claims 6, 11, and 21, recite limitations similar to those in Claim 1 discussed above. Therefore, all of Applicants' other independent claims, including Claims 6, 11, and 21, and all claims which depend from them, are

also patentable over the cited art, for similar reasons. Consequently, we request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 1, 3-6, and 8-26.

III. Claim Rejections Under 35 U.S.C. §103

Claim 27 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Dao in view of U.S. Patent Publication No. 2003/0028751 to McDonald et al. (“McDonald,” previously cited). Applicants respectfully traverse this rejection.

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants’ silence regarding any dependent claim is not to be interpreted as an agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION


In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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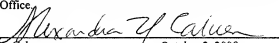
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.


Alexandra Y. Caluen October 2, 2008